CBCS Scheme

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15NT34

Third Semester B.E. Degree Examination, Dec.2016/Jan.2017
MOSFETS and Digital Circuits

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Discuss the type of MOS. **(06 Marks)**

b. What is JFET? Discuss the construction of JFET with neat diagram. **(04 Marks)**

c. Write a short note on second order effects in MOS. **(06 Marks)**

OR

2 a. Discuss the construction and characteristics of depletion type JFET. **(07 Marks)**

b. Discuss the VI characteristics of MOSFET. **(05 Marks)**

c. With the neat diagrams, explain twin well process. **(04 Marks)**

Module-2

3 a. Draw and explain realization of CMOS NOR gate and NAND gate. **(08 Marks)**

b. Discuss the delay parameters in CMOS. **(04 Marks)**

c. Write a note on AOI gate. **(04 Marks)**

OR

4 a. Explain the power dissipation equation for CMOS. **(06 Marks)**

b. Sketch and explain complementary CMOS gate computing $Y = \overline{(A + B + C) \cdot D}$. **(05 Marks)**

c. Write a note on MOSFET scaling and its impacts. **(05 Marks)**

Module-3

5 a. With a neat diagram, explain the operation of JK flipflop. **(06 Marks)**

b. Write a short comparison on latch versus registers. **(04 Marks)**

c. Define and explain the following terminologies setup time, hold time, clock to q delay, maximum clock frequency. **(06 Marks)**

OR

6 a. Explain CMOS master-slave register. **(06 Marks)**

b. Write a note on mux based latch. **(06 Marks)**

c. With neat diagram, explain the operation of D latch. **(04 Marks)**

Module-4

7 a. Define registers. Explain SISO and PIPO shift registers. **(05 Marks)**

b. Write a note on ring counter. **(05 Marks)**

c. Explain modulus-8 synchronous up/down counter with neat logic diagram. **(06 Marks)**

OR

8 a. Write a note on Johnson counter. **(05 Marks)**

b. Explain and design a mod-6 synchronous up counter using T flip-flop. **(07 Marks)**

c. Explain modulus-8 synchronous up counter with neat logic diagram. **(04 Marks)**

Module-5

9 a. Draw neatly and define Mealy and Moore machine model. **(06 Marks)**

b. Design a Mod-8 synchronous counter using JK flipflop to count number of occurrence of an input i.e. number of times it is 1. **(10 Marks)**

OR

10 a. Design a Mealy state diagram for the sequence 1101. **(06 Marks)**

b. Compare Mealy and Moore machine model and explain. **(06 Marks)**

c. Construct a state table for the following state diagram of Fig.Q10(c). **(04 Marks)**

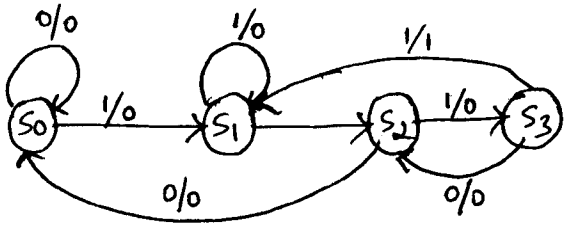

Fig.Q10(c)

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